Please add the following new claim:

32. (Added) The semiconductor structure of claim 31 wherein said electroplated conductive metal is about 4000 Å to about 30,000 Å thick.

## REMARKS

Claims 25-32 are now is the application. Claim 25 has been amended to clarify the location of the various layers. Claim 30 has been amended to address the rejection of 35 U.S.C. 112, first paragraph lowering the thickness of the copper seed layer.

The objection to the drawings has been obviated by the altered proposed changes to the drawings shown in red. The Specification has been amended to render it consistent with the amended drawings.

The rejection of claims 25-31 under 35 U.S.C. 112, second paragraph has been overcome by the above amendments to claim 25.

Claims 25-26 and 28-31 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,130,161 to Ashley, et al. Ashley, et al. fail to anticipate the present invention, since, among other things, Ashley, et al. do not disclose a conductive barrier located both over a major surface of the substrate and in recesses. The conductive barrier is located only in recesses as shown in the drawings of Ashley, et al. As discussed in the Specification, the presence of the conductive barrier over a major surface of the substrate is important to provide electrical contact for electroplating of the electroplated conductive metal. The structure of the present invention reduces subsequent polishing time for removing undesired plated metal overburden, along with minimizing the problem of "dishing." The structure of the present invention also minimizes erosion of the dielectric layer adjacent to isolated conductive features or regions.

Claims 25-26, 28-29 and 31 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,207,222 to Chen, et al. Chen, et al. fail to anticipate the

present invention since, among other things, Chen, et al. fail to disclose a structure whereby conductive barrier is located over a major surface of the substrate and in recesses along with the seed layer being located only in the recesses. Such structure is important to obtain the objectives discussed above.

Claims 25, 28, 29 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 5,821,168 to Jain. Jain does not anticipate the present invention since, among other things, Jain does not disclose a structure whereby the seed layer is located only in recesses. In particular, seed layer 60 in Jain is not restricted to recesses but is shown as being continuous over the entire surface in the figure therein. As discussed above, the structure of the present invention is important for obtaining the objections discussed above.

The rejection of claim 27 under 35 U.S.C. 103(a) as being unpatentable over Ashley, et al. is not deemed tenable. In particular, as discussed above, Ashley, et al. fails to disclose a conductive barrier located over a major surface of the substrate as required by the present invention.

Claims 27 and 30 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,207,222 to Chen, et al. Chen, et al. fail to render obvious claims 27 and 30. As discussed above, Chen, et al. do not disclose a structure whereby conductive barrier is located over a major surface of the substrate and recesses along with the seed layer being located only in the recesses.

Concerning the rejections under 35 U.S.C. 102, as discussed above, the cited references do not disclose each and every claim recitation. Accordingly, they fail to anticipate the present invention.

In particular, anticipation requires the disclosure, in a prior art reference, of each and every recitation as set forth in the claims. See *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985), *Orthokinetics, Inc. v. Safety Travel Chairs,*

*Inc.*, 1 USPQ2d 1081 (Fed. Cir. 1986), and *Akzo N.V. v. U.S. International Trade Commissioner*, 1 USPQ2d 1241 (Fed. Cir. 1986).

There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 USC 102. See *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (CAFC 1991) and *Studiengesellschaft Kohle GmbH v. Dart Industries*, 220 USPQ 841 (CAFC 1984).

In view of the above, consideration and allowance are, therefore, respectfully solicited.

In the event the Examiner believes an interview might serve to advance the prosecution of this application in any way, the undersigned attorney is available at the telephone number noted below.

The Director is hereby authorized to charge any fees, or credit any overpayment, associated with this communication, including any extension fees, to Deposit Account No. 22-0185.

Respectfully submitted,

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APPENDIX – MARKED UP VERSION

Page 7, first paragraph under "Best and Various Modes for Carrying Out Invention":

In accordance with the present invention, recesses 2 such as troughs and vias are provided on at least one major surface of a semiconductor substrate 13 [(not shown)]. Typical semiconductor substrates include silicon and group III-V semiconductors. Electrical insulation 3 is provided over the major surface and in the recesses such as silicon dioxide which can be thermally grown or deposited such as by chemical vapor deposition or physical vapor deposition. Typically, the insulating layer is about 2000 to about 30,000 Å thick, and more typically about 4000 to about 20,000 Å thick.

Page 13, first paragraph:

According to an alternative process according to the present invention, recesses 2 such as troughs and vias are provided on at least one major surface of a semiconductor substrate 13 [(not shown)]. Electrical insulation 3 is provided over the major surface and in the recesses such as silicon dioxide which can be thermally grown or deposited such as by chemical vapor deposition or physical vapor deposition. Typically, the insulating layer is about 2000 to about 30,000 Å thick, and more typically about 4000 to about 20,000 Å thick.

Claim 25:

25. (Amended) A semiconductor structure comprising a semiconductor substrate; recesses located in at least on major surface of said semiconductor substrate; electrical insulating layer located at least one major surface over said at least one major surface and in said recesses; a conductive barrier located over said insulating layer in said recesses and over said at least one major surface; a plating seed layer located over said conductive barrier within said recesses only; and an electroplated conductive metal in said recesses only.

Claim 30:

30. (Amended) The semiconductor structure of claim 28 wherein said copper is about 100 [4000] to about 2000 [20,000] Å thick.